GOA UNIVERSITY
Taleigao Plateau, Goa 403 206

RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2015

Course : Revised Course - 2013

COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 419 P R No : 201006303 Sex : M Name : TRAVASSO VALERIUS SIRUS

No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA
ASIC Design & FPGA					
	Theory	4	BB	P	
	IA	2	BB	P	
Digital Signal Processors & Embedded Systems					
	Theory	4	BB	P	
	IA	2	BB	P	
Design for Testability & E-Waste Management					
	Theory	4	BB	P	
	IA	2	BB	P	
Processor Architecture & Parallel Processing					
	Theory	4	CC	P	
	IA	2	BC	P	
Memory Design					
	Theory	4	BC	P	
	IA	2	BB	P	
Parallel Processing Lab					
	IA	2	BC	P	
	Practical	2	BB	P	
FPGA & Embedded Systems Lab					
	IA	2	AB	P	
	Practical	2	AA	P	
	Total :	38			6.74 P
					PASSES

Grade	Grade Points	Performance
AO	10	Outstanding
AA	9	Excellent
AB	8	Very Good
BB	7	Good
BC	6	Fair
CC	5	Satisfactory
FF	0	Fail

Read By : PPTalwe

Checked By : KM

Date : 18/3/16

S.S.J. Figueiredo
Assistant Registrar-E(Proff.)
18/3/2016

Leo V. Macedo
Controller Of Examinations
18/3/16

Prof. V.P. Kamat
Registrar
18.3.16

GOA UNIVERSITY TALEIGAO PLATEAU GOA

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average

Discrepancy, if any in the Result shall be informed to the University within a week from the date of receipt of the result by the college